REMARKS/ARGUMENTS

Claim 1 is amended by this response. Claim 10 is canceled. Accordingly, claims 1-9 and 11-20 remain pending.

Embodiments in accordance with the present invention relate to EEPROM devices and methods for manufacturing EEPROM devices, and in particular to EEPROM devices having a tunnel window provided in a stripe configuration.

Claims 1, 6, 8, and 9 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,273,923 to Chang et al. ("the Chang Patent"). Claims 3, 5, 7, and 10 were rejected as being obvious under 35 U.S.C. §103 in view of the Chang Patent. Claims 2 and 4 were rejected as being obvious in view of the Chang Patent considered in combination with U.S. Patent No. 5,293,331 to Hart et al. ("the Hart Patent"). Claims 11-15 and 17-20 were rejected under 35 U.S.C. § 103(a) as being obvious in view of the Hart Patent taken in combination with U.S. Patent No. 5,168,335 to D'Arrigo et al. (the D'Arrigo Patent). These claim rejections are overcome as follows

Regarding rejection of the claim set 1-9, Applicants have now amended claim 1, and the references relied upon by the Examiner, considered alone or in combination, fail to teach or even suggest an EEPROM integrated circuit structure as recited in claim 1 as amended. Specifically, the structure of claim 1 comprises a substrate including a surface region. A gate dielectric layer of a first thickness overlies the surface region of the substrate. A tunnel window provided in a stripe configuration is disposed within a portion of gate dielectric layer, the stripe portion extending across an entire length of a first cell region from a first isolation region to a second field isolation region, and to N other cell regions, N being greater than 2.

The Chang Patent discloses a tunnel area as an overlapped portion of a tunnel opening and an active region. The tunnel opening is provided in a slit configuration and the resulting tunnel area is substantially the configuration of a square (Figure 1). However, the tunnel window of the Chang Patent is not provided in a stripe configuration extended to other cell regions, as is recited in amended claim 1. Accordingly, claim 1 is patentable over the Chang Patent under 35 U.S.C. §102(b) at least for these reasons. Additionally, claims 2-10 and

additional features therein depending upon claim 1, should also be patentable for at least these and other reasons.

Regarding rejection of claims 11-20, in the latest office action the Examiner expressly acknowledged that the Hart Patent does not teach the tunnel oxide strip extending across an entire cell region from a first field isolation region to a second field isolation region, but asserted that such a feature is in fact taught by the D'Arrigo Patent.

However, referring to the D'Arrigo Patent (Figure 1 and col.. 3, lines 38-67), field isolation region is indicated by 24. By contrast, the oxide region 32 cited by the Examiner overlies a source region 30a and serves to define the lateral limits of channel regions 38a-b. Oxide region 32 cannot reasonably be understood to be a field isolation region, and thus the tunnel oxide window disclosed by the D'Arrigo Patent cannot reasonably be understood to extend from a first field isolation region to a second field isolation region as disclosed in claim 11. Accordingly, the Hart Patent in combination with the D'Arrigo Patent does not teach every feature of claim 11, and claim 11 is patentable over the cited references. Additionally, claims 12-20 and features therein depending from claim 11, should also be patentable for at least these and other reasons.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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